IN THE CLAIMS

Please amend the claims as follows:

1. - 2. (Canceled)

3. (Currently Amended) A circuit comprising:

a differential pair to receive a differential signal at a bulk input port and to generate an output signal at an output port and

further including a common source/drain terminal of the differential pair coupled to a current source, and wherein a common gate of the differential pair is biased to operate the differential pair in a saturation mode.

4. (Currently Amended) A circuit comprising:

a differential pair to receive a differential signal at a bulk input port and to generate an output signal at an output port, the differential pair having a biased common gate and configured to operate in a saturation mode, and

further including an amplifier coupled to the output port.

5. - 9. (Canceled)

10. (Currently Amended) A circuit comprising:

a differential pair configured to operate in a saturation mode and configured to receive a differential signal at a bulk input port and to generate an output signal at an output port and

further including an active load coupled to the drain output port and

wherein the active load includes a transistor pair having a common gate.

11. - 12. (Canceled)

13. (Currently Amended) A circuit comprising:

a first transistor having a first bulk and a first drain;

a first input node at the first bulk; and

a first output node at the first drain and

wherein the first transistor includes a first source to receive a bias current and wherein the first transistor is biased to operate in a saturation mode.

14. (Currently Amended) A circuit comprising:

a first transistor having a first bulk and a first drain;

a first input node at the first bulk; and

a first output node at the first drain and

wherein the first transistor includes a first source coupled to a supply voltage and wherein the first transistor is biased to operate in a saturation mode.

15.- 16. (Canceled)

17. (Currently Amended) A circuit comprising:

a first transistor having a first bulk and a first drain;

a first input node at the first bulk; and

a first output node at the first drain; and

and further including

a second transistor having a second gate in common with the first gate, the second transistor having a second bulk and a second drain;

a second input node at the second bulk; and

a second output node at the second drain and

wherein the first transistor and the second transistor are biased to operate in a saturation mode and include a common source.

18. (Original) The circuit of claim 17 further including a current source coupled to the common source/drain.

19. - 22. (Canceled)

23. (Currently Amended) A method comprising:

biasing a gate terminal of a first transistor in an amplifier, wherein the first transistor is operated in a saturation mode;

providing an input signal to a bulk terminal of the first transistor; and

generating a first output signal as a function of the input signal at a first output terminal coupled to a first drain terminal of the amplifier and

wherein providing the input signal includes providing a first differential input signal to the first transistor of a differential pair and providing a second differential input signal to a second transistor of the differential pair, and

further including biasing a source terminal of the first transistor.

24. (Original) The method of claim 23 wherein biasing the source terminal includes providing a current source.

25. - 26. (Canceled)

27. (Currently Amended) A communication device comprising:

an antenna having an antenna output;

a first amplifier including a transistor having a bulk terminal coupled to the antenna output and a bias node coupled to a gate terminal of the transistor wherein the transistor is operated in a saturation mode; and

a second amplifier having an input coupled to a first drain node of the first amplifier and wherein the bulk terminal is coupled to the antenna output via a tuner.

28. (Currently Amended) A communication device comprising:

an antenna having an antenna output;

a first amplifier including a transistor having a bulk terminal coupled to the antenna output and a bias node coupled to a gate terminal of the transistor wherein the transistor is operated in a saturation mode; and

a second amplifier having an input coupled to a first drain node of the first amplifier and further including a second source terminal of the transistor coupled to a power supply.

29. (Original) The device of claim 28 wherein the power supply includes a current source.

30. - 31. (Canceled)

32. (Currently Amended) A communication device comprising:

an antenna having an antenna output;

a first amplifier including a transistor having a bulk terminal coupled to the antenna output and a bias node coupled to a gate terminal of the transistor wherein the transistor is operated in a saturation mode; and

a second amplifier having an input coupled to a first drain node of the first amplifier and wherein the first amplifier includes a differential amplifier.

33. - 36. (Canceled)